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CMOS opened the door for many if not most of ... Another problem caused by excessive voltage is what is called “SCR Latchup”, basically an excessive voltage causes the PNPN junctions produced ...

*How CMOS Works: MOSFETs, JFETs, IGFETS And More*  
CMOS technology has evolved as the top choice for chip manufacturers ... This article refers to a feature size reduction topology and resulting degradation in latch-up performance. The article ...

*Latch-up Improvement For Tap Less Library Through Modified Decoupling Capacitors Cells*

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This is what is known as CMOS today. It draws almost zero static power dissipation ... so leakage currents are smaller. SOI devices have no latch-up problems. Drawbacks of SOI Devices: One of the ...

## *A Review Paper on CMOS, SOI and FinFET Technology*

Bipolar Summerland contrasted Bizen to bipolar technology, which has traditionally ... question that CMOS is flawed—although CMOS is prone to latch-up and ESD. CMOS is low power, has passed ...

## *Are Quantum-Tunnel Transistors Real, and What Do They Mean for Power Tech?*

A range of NXP Flip-Flops and

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Latches from the 74HC Family of CMOS Logic ICs. The 74HC Family use silicon gate CMOS technology to achieve operating speeds similar to the LSTTL family but with the low ...

*High-Speed CMOS Logic Latches*  
Single-ended Logic Signal I think of most logic as being in one of two major divisions as far as the technology used for today's logic: Bipolar and CMOS. Bipolar is characterized by use of ...

*Gates To FPGAs: TTL Electrical Properties*

Latch-up Current Limiters, multiple Interfaces and its unique CMOS space-qualified camera. Sierra Microwave supplied microwave communications

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NASA on Mars 2020/Perseverance  
Launch on Which 3 HEICO  
Subsidiaries Supplied Critical  
Hardware*

In the early days of solid-state logic gate circuit technology, there was a very clear distinction between TTL and CMOS. TTL gates were capable of switching on and off very fast, required a tightly ...

## *CMOS Logic Gates*

Thanks to its ultra-thin body and buried oxide, by construction the FD-SOI technology exhibits high resilience against radiation errors, such as bit flip or latch-up,

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## *Efficiency at All Levels*

“You have a lot of very large technology companies ... The company’s Smart Backplane mitigates single-event latchup by detecting changes in the current into an embedded computing module.

## *Radiation tolerance meets commercial space*

Some of the inherent properties in favour of SOI technology over bulk include the reduction of junction capacitance, the ease to make shallow junctions, radiation hardness, and latch-up immunity [1 ..

## *Chapter 8: Silicide Technology for*

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Passive isolation addresses effects such as single-event latchup ... part radiation hardness as process technology advances. As an example, deep-submicron CMOS processes have very thin gate ...

## *Commercial Satellite Programmes Drive Rad-Hard Technology Evolution*

This class provides for active solid-state electronic devices, that is, electronic devices or components that are made up primarily of solid materials, usually semiconductors, which operate by the ...

**CLASS 257, ACTIVE SOLID-STATE  
DEVICES (E.G., TRANSISTORS,**



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Thanks to its ultra-thin body and buried oxide, by construction the FD-SOI technology exhibits high resilience against radiation errors, such as bit flip or latch-up, bringing additional reliability ...

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